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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,680	12/16/2003	Takahito Nakano	246575US6	3581

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,680	NAKANO ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4 – 5, and 7 – 9 have been examined.

Response to Arguments

2. Applicant's arguments filed 05 June 2006 have been fully considered but they are not persuasive.

As per the rejection to claim 1, Applicant argues that the cited reference, US Patent No 6,889,299 (hereinafter Yamada), does not teach a "semiconductor information output means that comprise connection control means for controlling a read out operation of a program stored on an external storage means, wherein the program is used for executing the read out operation of the semiconductor information" (emphasis in original) (See remarks; Page 9). Applicant also argues that Yamada does not teach a "semiconductor information output means that comprise control means for controlling the read-out operation and external operating operation of the semiconductor information based on the read-out program read by the connection control means" (emphasis in original) (See remarks; Page 9).

The Examiner submits that Yamada does teach the claim limitations recited above. Yamada teaches semiconductor information output means (Figure 9 Item 62) that comprise connection control means (Figure 9 Item 62) for controlling a read out operation of a program (Col 8 Lines 58 – 60 "address data") stored on an external storage means (Figure 9 Item 63), wherein the program is used for executing the read out operation of the semiconductor information (Col 8 Lines 23 – 29). The address

stored in the register tells the ID Write Circuit (Figure 9 Item 62) where to write the ID in the external memory (Figure 9 Item 212). Yamada also teaches a semiconductor information output means that comprise control means for controlling the read-out operation and external operating operation of the semiconductor information based on the read-out program read by the connection control means. The ID is stored at an address specified by the Address Register For Writing ID (Figure 9 Item 63, Col 8 Lines 55 – 58).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4 – 5, and 7 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No 6,889,299 (hereinafter Yamada).

As per claims 1, 5, and 8, Yamada teaches a semiconductor integrated circuit apparatus mounted on a predetermined circuit board, the apparatus comprising semiconductor information storage means (Figure 9 Item 61) for storing semiconductor information unique to the semiconductor integrated circuit apparatus (Col 8 Lines 49 – 53); and semiconductor information output means (Figure 9 Item 62) connected to the

semiconductor information storage means for reading out the semiconductor information from the semiconductor information storage means in response to an externally supplied signal (Col 8 Lines 49 – 53 "reset signal input through a terminal 64 and a command end signal input through a terminal 65") and outputting the read-out semiconductor information (Col 8 Lines 49 – 58), wherein the semiconductor information output means includes connection control means (Figure 9 Item 62), which is configured to be connected to external storage means (Figure 9 Item 63) storing a program (Col 8 Lines 58 – 60 "address data"), for controlling a read-out operation of the program stored in the external storage means (Col 8 Lines 23 – 29), the program being used for executing the read-out operation of the semiconductor information (Col 8 Lines 23 – 29), and control means (Figure 9 Item 62) for controlling the read-out operation and external outputting operation of the semiconductor information based on the read-out program read by the connection control means (Col 8 Lines 55 – 58).

As per claim 4, Yamada also teaches wherein the semiconductor information storage means (Figure 9 Item 61) stores an identification code (Col 8 Lines 49 – 53) as the semiconductor information, the identification code being assigned to allow identification of the semiconductor integrated circuit apparatus (Col 6 Lines 29 – 32), and outputs an electric signal according to the identification code in response to an input of a read-out signal (Col 8 Lines 49 – 53).

As per claim 7, Yamada teaches writing a program (Col 8 Lines 62 – 63), which is for reading out semiconductor information unique to the semiconductor integrated circuit apparatus and stored in the semiconductor integrated circuit apparatus, into a predetermined external storage means (Figure 9 Item 63); reading the program written into the external storage means and reading out the semiconductor information based on the read program (Col 8 Lines 55 – 63); and writing the read-out semiconductor information into a predetermined region of the external storage means (Figure 9 Item 212; Col 8 Lines 58 – 63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,889,299 (hereinafter Yamada) in view of US Patent No. 5,856,923 (hereinafter Jones).

As per claim 9, Yamada teaches the apparatus as described per claim 7 (see rejection of claim 7 above). Yamada also teaches wherein the semiconductor information includes a production history (product version, for example), a manufacturer's number, or the like of the IC chip (Yamada; Col 4 Lines 15 – 20).

Yamada does not teach wherein the semiconductor information includes at least one of a wafer number, information of a position on a wafer, and a manufacture time of the semiconductor integrated circuit.

However, Jones teaches a semiconductor ID code that is specified by a lot number, wafer number, and wader position for the IC device (Jones; Col 4 Line 66 – Col 5 Line 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Yamada to include the ID code because doing so allows for correlations to be found between process variables, such as the processing equipment used, and performance variables, such as test results (Jones; Col 5 Lines 25 – 27).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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8/7/2006